A Six Million Pixel Full-Frame True 2 f CCD Image Sensor Incorporating Transparent Gate Technology and Optional Antiblooming Protection

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ABSTRACT

This paper describes the performance of an advanced high-resolution full-frame architecture CCD imaging device for use in scientific, medical, and other high performance monochromatic digital still imaging applications. Of particular interest is the replacement of the polysilicon 2nd gate electrode with that of a more spectrally transparent material, thereby dramatically improving device sensitivity. This has been achieved without compromising performance in other areas such as dark current, noise, transfer efficiency and, most importantly, yield. Devices have also been produced with and without antiblooming protection depending on an application's primary need for sensitivity or control of over-exposure conditions.

Keywords: CCD, Image Sensor, Transparent Gate, Full-Frame, Antiblooming

1. INTRODUCTION

A great many high-end imaging applications today utilize large format full-frame and frame-transfer style CCD image sensors. The benefits of this architecture are the high sensitivity, high charge capacity and low dark currents resulting in very large dynamic ranges. Because of the relative simplistic nature of the design, very large format sensors have been manufactured at reasonable cost. Typical devices in this class are front-side illuminated and tend to have lower sensitivity (or quantum efficiency—QE) for wavelengths less than 500 nm. The major contributor to sensitivity loss is the overlying polysilicon gate electrode structures, which tend to absorb or reflect incident light depending on wavelength. To circumvent this problem, backside illuminated, UV-sensitive phosphor overlay and virtual phase technologies, among others, have been developed.[1]

Backside thinning processes circumvent the polysilicon gates by sensing light from the back of the silicon substrate. In this case, the thick (~500-600 μm) silicon substrates are first reduced to a thickness of ~10 μm in order for the electric fields to 'pull' higher energy (shorter wavelength) induced electrons into the buried channel collection regions. The resulting QE can approach unity for some wavelengths. Thinning processes, however, are very complex and tend to limit themselves to very high performance, low volume applications. UV-sensitive phosphors are special coatings deposited onto the device's surface. These coatings absorb photons in the 200-450 nm range and emit photons at ~550 nm. Above 450 nm, the coatings become transparent. The QE improvement tends to be limited to ~10-15% and the coatings tend to degrade uniformity, cosmetic quality, and to some extent MTF (especially as the pixel size decreases). Virtual or open pinned phase technology replaces polysilicon gates with an open 'phase' where additional ion implantation steps are required to create proper pixel isolation. Here the advantage is that the open phase has less optical restrictions into the substrate—much like the backside system. The drawbacks of this technology in the past have included higher clock swings, charge transfer inefficiency and noise.

This paper describes a new class of full-frame CCD where the second level of polysilicon gate electrodes have been replaced with a more optically transparent conducting gate material made of indium-tin-oxide or ITO.[2] This processing technology has been further developed, which maintains the simplicity and high yield (low cost) of front illuminated CCDs while at the same time providing significant improvements in shorter wavelength QE. It enables an intermediate cost versus performance choice between current front and back illuminated designs. This technology is applicable to all Kodak full-frame sensors including the *Kodak Digital Science*™ KAF-6303E 3k x 2k image sensor, which serves as the basis for this paper. A derivative of this device has also been manufactured called the *Kodak Digital Science*™ KAF-6303LE image sensor, which contains an antiblooming drain to control over exposure conditions. A description of the architecture is given followed by performance measurements made to date.

2. ARCHITECTURE

The KAF-6303E/LE sensor devices are built using heavily doped p-type substrates with a more lightly doped p-type epitaxial layer on top. N-channel transistors and shift registers are built using a single level of doped polysilicon and a single level of ITO gate electrodes. A single level of aluminum connects the gates to bonding pads. Buried channel vertical CCD shift registers are formed, which serves as both the integrating photoactive region and for parallel (line by line) readout of the pixels. A horizontal register accepts each line from the vertical register, one at a time, and shifts pixels to a single output node in a serial fashion. The output node converts the electrons into a voltage, which can be processed and digitized. The total device area measures 29 x 19.1 mm and is housed in a 26-pin DIL ceramic package. A general architecture drawing of the device is shown in Figure 1.

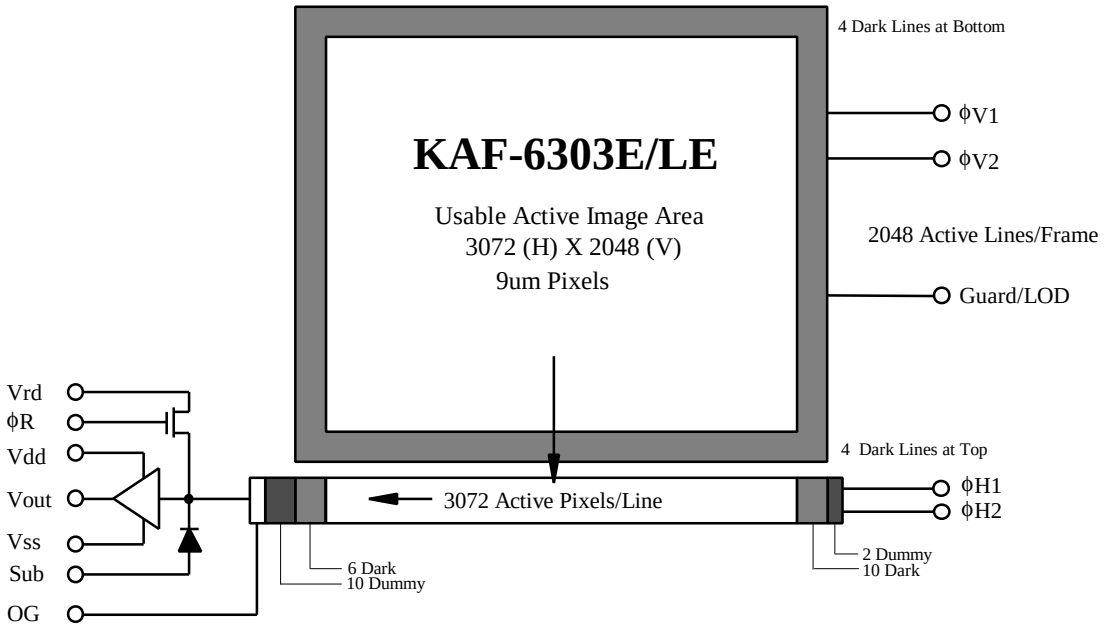


Figure 1. KAF-6303E/LE sensor function diagram.

2.1 Pixel Architecture

The pixel design of the KAF-6303E and KAF-6303LE image sensors employs a true 2ϕ architecture[3] and a simplified schematic of the layout is shown in Figure 2. It is 9 μm on a side and contains two gates per pixel, which are called ϕ1 (made from polysilicon) and ϕ2 (ITO). The ITO material has simply replaced the area previous occupied by a second level of polysilicon. Horizontal running barrier regions are implanted under a portion of each gate, which enables proper vertical isolation of pixels during integration and readout. A field or channel stop region runs vertically that ensures horizontal isolation. 100% of the pixel is photoactive for the KAF-6303E sensor and the linear (to 1%) charge capacity has been measured to be typically 95ke- (95,000 electrons). In the case of the KAF-6303LE sensor, additional barrier regions and a lateral overflow drain (LOD) are defined. These features have the ability to limit the amount of charge integrated into each pixel site via an LOD channel located in ϕ2. The tradeoffs for this added feature are reduced photosensitive fill factor (70%) and linear charge capacity (54ke-) caused by a smaller effective pixel size. The lower fill factor inherently reduces quantum efficiency as well. There are 3072 x 2048 photoactive pixels in each row. Additional dark reference rows and columns are added along each edge as shown in Figure 1.

The true 2ϕ architecture is a highly manufacturable process from a yield perspective. Because each level of conductor (ϕ1 and ϕ2) is driven with the same clock, inter-level shorts are not fatal; rather cosmetic defects are created, which can be still acceptable depending on the application and cost requirements. A ϕ1 to ϕ1 short is likely to cause column defects while ϕ2 to ϕ2 shorts appear more like a point or cluster defect.

As pixel sizes shrink, the true 2ϕ process provides less demanding requirements on photolithography than 3 or 4 phase devices. One drawback to the architecture lies in the fixed channel potential difference between barrier and storage regions within a pixel. The process essentially fixes this capacity and clocking levels will have little effect of increasing or decreasing this amount.

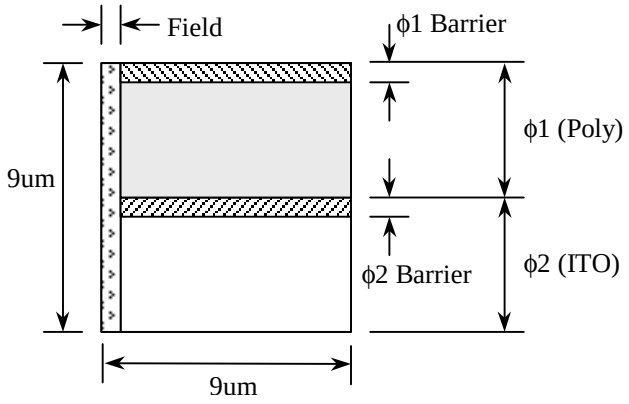


Figure 2a. KAF-6303E sensor pixel architecture.

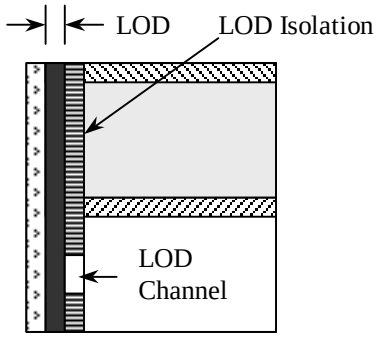


Figure 2b. KAF-6303LE sensor pixel architecture.

2.2 Shift Register Operation

During integration, both phases are held in accumulation with a negative voltage as represented in Figure 3a. Following integration, charge from both phases is recombined into ϕ1 by applying a positive voltage on ϕ1 (3b). The voltage polarities of ϕ1 and ϕ2 are reversed to transfer charge from ϕ1 to ϕ2 (3c). Switching the voltages of both phases again push charge from ϕ2 to ϕ1 of the next pixel (3d). The cycle completes when ϕ1 returns to accumulation with a negative voltage (3e). At this point a line of charge has been presented to the horizontal register that transfers charge in traditional complementary clocking to the output. This method of clocking is commonly referred to as MPP[4] or accumulation mode and was first introduced by Saks.[5] By maximizing the amount of time the gates are held with a negative voltage, the dark current generation rate is greatly reduced. The negative voltage on the gates causes holes to accumulate near the oxide/silicon surface. These holes neutralize (recombine) unwanted electrons which are emanating from this interface leaving only the depletion and bulk components of device dark current.

Unlike many designs, the true 2ϕ architecture of this device is able to implement MPP mode without degradation of charge capacity. It works by building in an offset difference in the barrier potentials of each phase relative to one another while in the accumulated state. During the last cycle of MPP mode (Figure 3e) the charge capacity under ϕ1 begins to collapse. Because the barrier potential under ϕ1 is slightly deeper than ϕ2, excess charge is always preferentially spilled backwards into the adjacent ϕ2 thereby increasing overall pixel capacity.

The dashed lines in Figure 3 represent the potential level at which the LOD channel resides (KAF-6303LE version only). If the signal value under any particular gate reaches that value, charge spills from the pixel into the LOD region, which will then be removed off chip before it can spill into an adjacent pixel. In contrast to vertical overflow drain (VOD) architectures,[6] the lateral overflow drain design measures good linearity up to >90% (~75% for VOD) of the pixel's saturation value at the expense of lower fill factor. LOD's will maintain better QE in wavelengths >550nm compared to VODs because the deep depletion region beneath the pixel is preserved.

3. PERFORMANCE

In the following sections, key performance metrics are evaluated and compared against traditional double level polysilicon and ITO second gate-based processes. These include the quantum efficiency, dark current, linearity, and antiblooming. Other performance parameters have been confirmed not to vary with process/design differences.

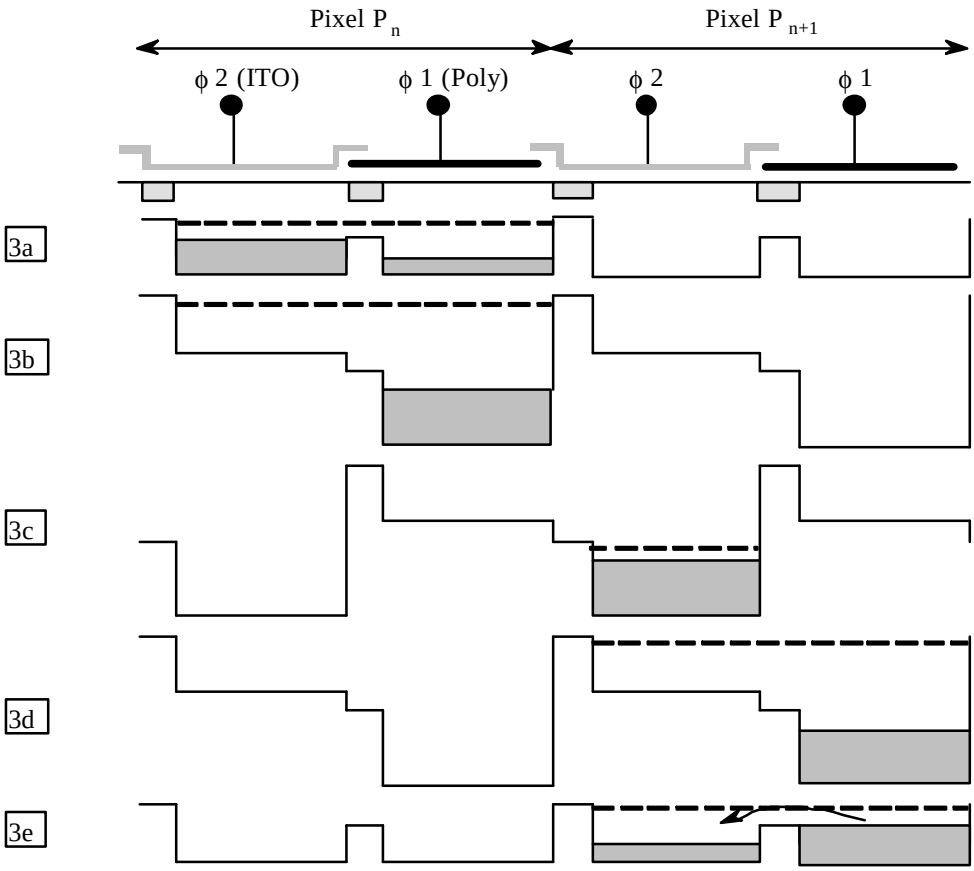


Figure 3. Vertical shift register operation.

3.1 Quantum Efficiency Measurements

Quantum Efficiency (QE) or spectral response is the number of electron-hole pairs (e-) created and successfully readout of the device for each incoming photon. It is represented as a percent or in terms of e-/photon. In simple silicon based imaging, it can never exceed 100% efficiency.

The QE of the ITO and polysilicon devices are measured as a function of wavelength from 370 to 1100nm. Current equipment capability prevents measuring below 370nm at this time. In Figure 4, the QE of the KAF-6303E sensor (ITO process) is compared to that of the KAF-6303 sensor (double poly process). The ITO process, due to it's better transmission properties, is clearly superior at wavelengths less than ~750nm with an improvement of ~10x at 400nm (from 3% to 30%). At wavelengths above ~750nm, there is little difference in the designs because of photons being absorbed much deeper into the silicon where there are less electric fields available to collect the signal. The theoretical limit at which the photons appear transparent to the silicon is ~1100nm. Figure 5 represents a similar analysis for the pixel design with an LOD for antiblooming protection. In this case, the gain again is ~10x (from 1.5 to 18%) and the QE has dropped primarily because of the amount predicted by the fill factor difference. Depletion regions generated from biasing the LOD structure tend to contribute to additional QE losses.

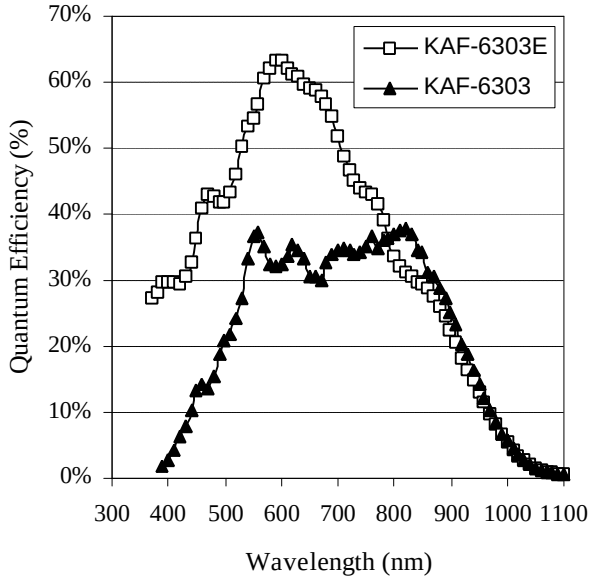


Figure 4. Quantum efficiency (non-LOD design).

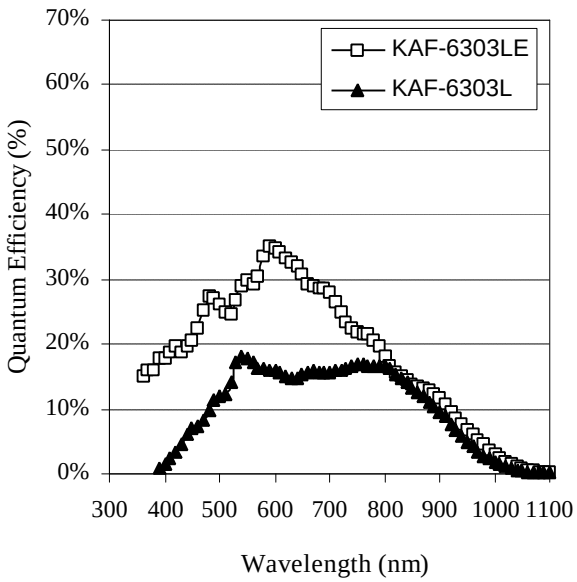


Figure 5. Quantum efficiency (LOD design).

3.2 Dark Current Measurements

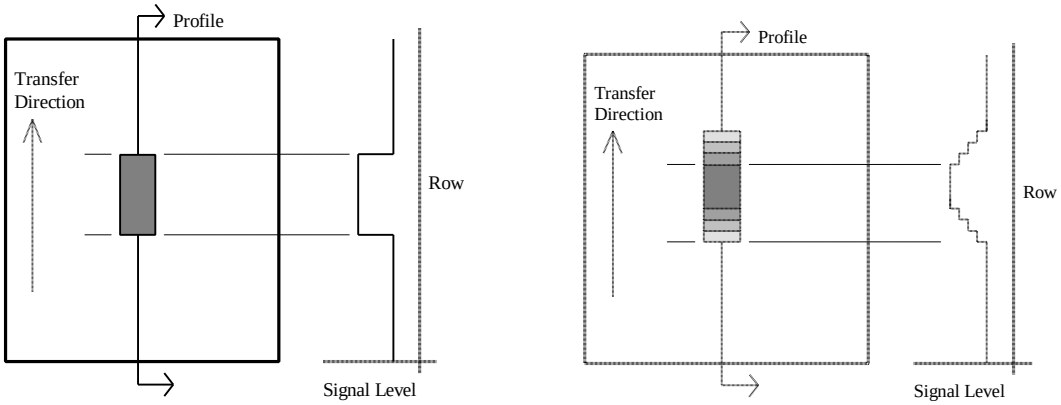
The dark current in a device represents an offset in the signal level measured in the absence of any light. It is typically specified as an average value for all pixels. The average dark current, however, is rarely a concern in an imaging system because this value can be easily removed either in the analog or digital domain. The exception to this is if the level is so high that the loss in effective charge capacity drops below required levels. Instead, it is the variability of the dark current in each pixel that degrades image quality. Dark current noise will degrade image quality by either (1) a fixed pattern non-uniformity from pixel to pixel or (2) as a shot noise component where the value in each pixel varies from frame to frame depending on the level of the average dark current level of that pixel. Dark current will vary strongly depending on temperature level. As the temperature increases, the energy/mobility of electrons in the valence band increases, thereby improving chances of a transition into the conduction where it becomes free to be collected and sensed by the device.

The dark current has been measured at several temperatures for the KAF-6303E/LE sensor device. The dark current generation rates between the poly and ITO processes are essentially the same within the tolerance of lot to lot variations. At room temperature, the typical dark current for the non-LOD design is 3.5 pA/cm^2 whereas that of the LOD design is 2.4 pA/cm^2. The difference, again, is mainly due to the fill factor difference where the LOD bias drains dark signal immediately off the chip before it can reach the buried channel. The temperature dependence has been found to double the dark current for every 5-6^{o}C increase.

3.3 Photon Transfer Measurements and the Delayed Exposure Linearity Test Method

Imaging with a CCD device is an inherently linear process. It is primarily limited by the linearity of the output amplifier and the charge transfer efficiency (which commonly exceeds 99.9995% efficiency per gate transfer depending on frequency). This provides very precise measurements of light quanta—both in signal intensity level and geometric arrangement. Janesick, et al. have devised an absolute method to measure or calibrate a CCD for linearity in addition to providing values for system noise, charge-voltage conversion gain, and full-well charge capacity. This method is called the Photon Transfer Technique.[7] It utilizes the fact that the amount of rms noise associated with an exposure level of photons is exactly equally to the square root of the average value provided sufficient sample points are available.
The measurement technique used for the ensuing performance parameters was generated with a modified approached to the Photon Transfer method. Rather than capturing multiple frames to determine each data point in the curve, the entire curve can be constructed with only one or two captures using a delayed exposure technique. Referring to Figure 6, the principle is to

expose the device while the vertical shift register has already begun shifting charge to the output—similar to time delay and integration (TDI) imaging. As lines are clocked out of the device (or under the light shielded rows), they no longer receive additional exposure. The first line out will have one line time of exposure, the second will have two and so forth. A convenient illumination source for this test is LEDs where the light can be precisely gated and synchronized to line times. The resulting vertically 'smeared' image contains a linear ramp (both up and down in signal levels), which can then be analyzed for photon statistics on a line-by-line basis. In practice, it is difficult to precisely focus object edges on the device to know where the ramp begins or ends. By using dark reference rows (either leading or trailing) built into the device with a flat field exposure enables a more controlled and production test worthy feature. Typically, the trailing edge is used that will fold vertical transfer inefficiency effects into the ramp data. Using the trailing edge also requires the system to clock and capture additional lines through the array than would normally be done. The number of data points in the curve is determined by the number of line times the exposure is overlapped into the readout. By increasing or decreasing light intensity levels (again LEDs make this convenient), the resolution between data points can made coarse or fine—even down to the electron per point levels. Aside from significant reduction in measurement times, this method also reduces errors caused by low frequency drifts in electronics or exposure conditions.



*Note: The dark rectangle represents a focused object on the CCD.

Figure 6a. Standard exposure and readout.

Figure 6b. Delayed exposure timing.

3.3.1 Charge capacity and low level nonlinearity

The charge capacity is evaluated by determining the point along the linearity curve (signal vs exposure), which deviates by a pre-determined percentage (typically 1%) from a straight line. The straight line is determined as the least squares linear fit to the central values of the curve. Using the only the center values allows each end to 'float' thereby highlighting problems at the high or low end of the signal range. The 1% linear saturation voltage of the KAF-6303E typically measures 95ke- and the KAF-6303LE sensor measures 54ke-. For the KAF-6303LE sensor this represents 94% of the saturated signal (57ke-).

The low signal level nonlinearity is defined as the Y-axis intercept (Yint) from the straight line fit as described in the preceding paragraph. It is measured in units of DN or mV. As linearity degrades, the value of Yint deviates from 0. Percentages are avoided at the low end where signal levels are very small and measurement noise becomes to dominate. The Yint of the KAF-6303E/LE sensor devices has been measured to be typically -2.3 mV when using the central ¼ points for the least squares fit of the linearity curve. Figure 7 contains an example of this method using a device with the LOD structure.

3.3.2 Charge to voltage conversion gain

Referring to Janesick,[7] et al., the conversion gain is determined by calculating the slope of the mean signal level versus the variance (once system offsets are removed) using digital counts (DN) from the analog to digital converter. Instead of determining these values from a subsection within the array, the measurements come from single lines within the ramp. The inverse slope represents the conversion gain in units of e-/DN. Knowing the system gain (V/DN) provides units of V/e-. For the KAF-6303E/LE sensor device, this results in ~10 μV/e-. See Figure 8.

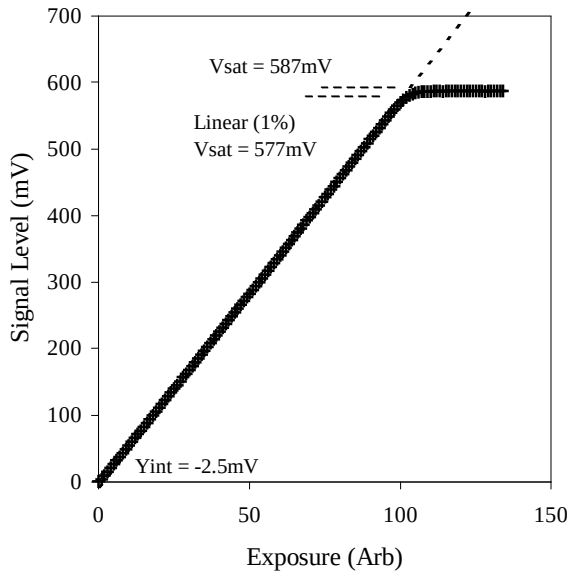


Figure 7. Signal vs exposure using delayed exposure method (LOD device).

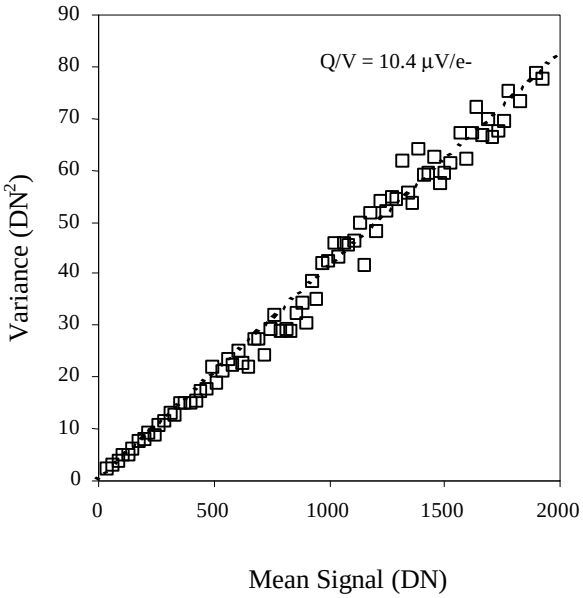


Figure 8. Mean-variance plot to determine charge-to-voltage conversion.

3.3.3 Noise and dynamic range

The noise in a CCD tends to be dominated by the on-chip amplifier. Because the transistors of the KAF-6303E/LE devices are all made using the first level of polysilicon, we expect the noise to be independent of the ITO or double polysilicon processes. As the mean signal level decreases in the photon transfer curve, the readout noise of the sensor and electronics dominate. The lowest noise value acquired represents the total noise. To obtain the sensor noise, the CCD's output is disconnected to the signal processing, which yields the electronic noise caused by the system. This total value is discounted by the system noise (in quadrature) and the KAF-6303E/LE sensor yields a sensor noise of ~15e- rms.

The dynamic range is defined as the charge capacity divided by the sensor noise. For the KAF-6303E sensor devices this amounts to 76 dB or 12.6 bits. The KAF-6303LE sensor provides 71dB or 11.8 bits.

4.3 Antiblooming

Antiblooming is a term used to describe the ability of a CCD image sensor to handle overexposure conditions. Devices designed without any antiblooming capability will spill charge into adjacent (usually vertically) pixels when exposed to a level exceeding the pixel charge capacity causing false readings. Measurement of antiblooming performance is similar to linearity measurements in that it's not universally consistent. A typical method (common among interline devices) is to illuminate a spot that is 10% of the vertical height of the imager. The protection factor, in terms of multiples above the linear saturation exposure point, occurs when columns in-line with the spot are saturated as well. For this class of device that would not typically occur until 1000x or more. In practice, lens flare becomes substantially more objectionable before this limit is achieved. Measurements have been made which confirm that this design exceeds at least 128x saturation. Images showing devices with and with antiblooming protection in response to a 24x over-exposure conditions are shown in Figure 9.

4. SUMMARY

A six million pixel CCD imaging device has been developed using ITO transparent gate technology. This technology significantly improves quantum efficiency at wavelengths below 750nm, while maintaining similar performance between 750 and 1100 nm. This has been achieved without adding additional complexity to the manufacturing process or degrading other

performance aspects of the device compared to the traditional double polysilicon process. These devices join a family of full-frame devices now being produced using this technology (see Table 1).

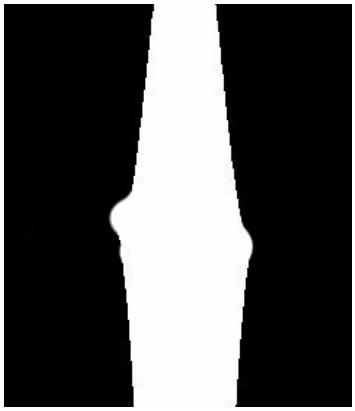


Figure 9a. KAF-6303E sensor at 24x saturation exposure.

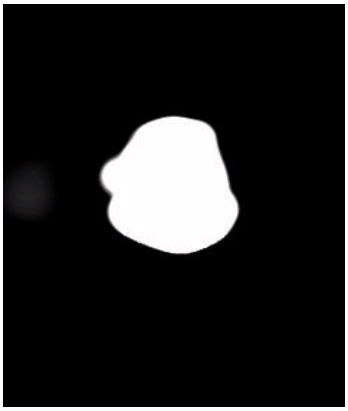


Figure 9b. KAF-6303LE sensor at 24x saturation exposure.

Sensor Device	Pixels	Pixel Size	Antiblooming
KAF-0261E	512 x 512	20 μm	No
KAF-0401E	768 x 512	9 μm	No
KAF-0401LE	768 x 512	9 μm	Yes
KAF-1001E	1024 x 1024	24 μm	No
KAF-1301LE	1280 x 1024	16 μm	Yes
KAF-1401E	1320 x 1035	6.8 μm	No
KAF-1602E	1536 x 1024	9 μm	No
KAF-1602LE	1536 x 1024	9 μm	Yes
KAF-6303E	3072 x 2048	9 μm	No
KAF-6303LE	3072 x 2048	9 μm	Yes

Table 1. Full-Frame CCDs from Kodak employing ITO transparent gate technology.

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REFERENCES

1. Gerald C. Holst, "*CCD Arrays, Cameras and Displays*," pp. 92-96, SPIE and JCD Publishing, 1996
2. S. L. Kosman, E. G. Stevens, J. C. Cassidy, W. C. Chang, P. Roselle, W. A. Miller, M. Mehra, B. C. Burkey, T. H. Lee, G. A. Hawkins and R. P. Khosla, "A Large Area 1.3-Megapixel Full-Frame CCD Image Sensor with a Lateral-Overflow Drain and a Transparent Gate Electrode," *IEDM Technical Digest*, pp. 287-290, 1990.
3. E. G. Stevens, T. H. Lee, D. N. Nichols, C. N. Anagnostopoulos, B. C. Burkey, W-C Chang, T. M. Kelly, R. P. Khosla, D. L. Losee and T. J. Tredwell, "A 1.4-Million-Element CCD Image Sensor," *ISSCC Technical Digest*, pp. 114-115, 1987.
4. J. Janesick, T. Elliot, "History and Advancements of Large Area Array Scientific CCD Imagers," Astronomical Society of Pacific Conference Series, Tucson, AZ, 1991.
5. N. S. Saks, "A Technique for Suppressing Dark Current Generated by Interface States in Buried Channel CCD Imagers," *IEEE Electron Device Letters*, EDL-1, No. 7, pp. 131-133, July 1980.
6. D. N. Nichols, W.-C. Chang, B. C. Burkey, E. G. Stevens, E. A. Trabka, D. L. Losee, T. J. Tredwell, C. V. Stancampiano, T. M. Kelly, R. P. Khosla, T. H. Lee, "A 1.4-Million-Element, Full Frame CCD Image Sensor with Vertical Overflow Drain for Antiblooming and Low Color Crosstalk," *IEDM Technical Digest*, pp. 120-123, 1987.
7. J. Janesick, K. P. Klaasen, T. Elliot, "Charge-Coupled-Device Charge-Collection Efficiency and the Photon-Transfer Technique," *Opt. Eng.*, 26, No. 10, pp. 972-980, 1987.